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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/063,788 | 05/13/2002 | Yoshitami Sakaguchi | JP920010105US1 | 1629 |

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| EXAMINER | |
|---|---|
| SHANKAR, VIJAY | |
| **ART UNIT** | **PAPER NUMBER** |
| 2673 | |

DATE MAILED: 12/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/063,788 | SAKAGUCHI ET AL. | |
| | Examiner | Art Unit | |
| | VIJAY SHANKAR | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-12,19 and 20* is/are allowed.

6)☒ Claim(s) *1-7,9 and 13-18* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 9, and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakaguchi et al (6,806,861) in view of Buhr et al (5,528,339).

Regarding Claims 1, 4, Sakaguchi et al teaches a liquid crystal display, comprising liquid crystal cells forming an image display area on a substrate (Col.2, line 56- col.3, line 62); and a driver for applying a voltage to the liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein the driver keeps a number of switching times for pulse strings per time unit constant for a predetermined range of the digital input data when generating the pulse strings with pulse densities corresponding to the digital input data (Figures 1-6, 10-14; Col.3, line 8- Col.4, line 59; Col.5, line 60- Col.6, line 7, line 56).

However, Sakaguchi et al does not teach a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data.

Buhr et al teaches a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data (Figures 3-4,9,11; Column 6, line 8- Col.7, line 52; Col.8, line 15- 65) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Buhr et al into Sakaguchi et al for providing the natural image reproduction.

Regarding Claims 2-3, Sakaguchi et al teaches the liquid crystal display wherein the driver is mounted on the substrate and is comprised of a plurality of driver ICs connected via signal lines; and the predetermined range of the digital input data is a predetermined range around a medium value of the digital input data (Col.7, line 7-56).

Regarding Claim 5, Sakaguchi et al teaches a liquid crystal display, comprising: liquid crystal cells forming an image display area on a substrate (Col.2, line 56- col.3, line 62); and a driver for applying a voltage to the liquid crystal cells based on a reference voltage for gamma correction corresponding to digital input data, wherein the driver obtains an output voltage using pulse density modulation (PDM) (Col.3, line 8-64; Col.5, line 61- Col.6, line 56) as well as obtains an output voltage using pulse width modulation (PWM) (Col.3, line 8-64; Col.5, line 61- COl.6, line 56) for a predetermined range of the digital input data around a medium value when generating pulse strings corresponding to the digital input data. (Figures 1-6, 10-14; Col.3, line 8- Col.4, line 59; Col.5, line 60- Col.6, line 7, line 56).
However, Sakaguchi et al does not teach a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data.

Buhr et al teaches a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data (Figures 3-4,9,11; Column 6, line 8- Col.7, line 52; Col.8, line 15- 65) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Buhr et al into Sakaguchi et al for providing the natural image reproduction.

Regarding Claims 6,7,9, Sakaguchi et al teaches a liquid crystal display driver for applying a voltage to liquid crystal cells forming an image display area, comprising: a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted (Col.5, line 60- Col.6, line 35); and a pulse select/synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and the reference pulses, wherein the pulse generation circuit generates the reference pulses without changing a number of switching times per time unit for a predetermined range of the digital input data around a medium value. (Figures 1-6, 10-14; Col.3, line 8- Col.4, line 59; Col.5, line 60- Col.6, line 7, line 56).

However, Sakaguchi et al does not teach a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data.

Buhr et al teaches a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data (Figures 3-4,9,11; Column 6, line 8- Col.7, line 52; Col.8, line 15- 65) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Buhr et al into Sakaguchi et al for providing the natural image reproduction.

Regarding Claims 13-18, Sakaguchi et al teaches a reference pulse generation circuit for digital-analog conversion employing a pulse density modulation scheme (Col.5, line 60- Col.6, line 35), comprising: means for generating reference pulses that are exclusively in a high state corresponding to digital input data (Col.3, line 8- Col.4, line 65; Col.5, line 60- Col.6, line 35); and means for generating the reference pulses such that a number of switching times for pulse strings per time unit is constant for a predetermined range of the digital input data around a medium value. (Figures 1-6, 10-14; Col.3, line 8- Col.4, line 59; Col.5, line 60- Col.6, line 7, line 56).
However, Sakaguchi et al does not teach a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data.

Buhr et al teaches a liquid crystal display comprising the digital input data, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data (Figures 3-4,9,11; Column 6, line 8- Col.7, line 52; Col.8, line 15- 65) .

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have incorporated the teaching of Buhr et al into Sakaguchi et al for providing the natural image reproduction.

***Allowable Subject Matter***

4. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Claims 10-12 and 19-20 are allowed.

6. The following is an examiner's statement of reasons for allowance: The present invention is directed to a liquid crystal display driver wherein the pulse select/ synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of the pulse generation circuit where m=n-W and the digital input data D(m-1) through D(O) as claimed in Claim 8.

The present invention is directed to a reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, comprising: an n-bit binary counter for counting up in synchronization with an input clock; an n-1 bit latch for generating signals by delaying high order n-1 bits output B (n-1) through B(1) from the binary counter by one input clock period; and n-1 logical circuits for performing logical operations with receiving as inputs the high order n-1 bits output B(n-1) through B(1) from the binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from the n-1 bit latch and obtaining outputs X(0) through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained bypassing the logical circuit, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data, and wherein the n-1 logical circuits are n-1 AND circuits, and the n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3) and a NOR circuit outputting X(n-2) ad claimed in Claims 10-12.

The present invention is directed to a liquid crystal display driver for applying a voltage to liquid crystal cells forming an image display area comprising: a pulse generation circuit for generating a plurality of reference pulses in which pulse generation densities are weighted; a pulse select/ synthesis circuit for generating a pulse string by selecting and synthesizing necessary reference pulses on the basis of digital input data and the reference pulse wherein the pulse generation circuit

generates the reference pulses without changing a number of switching times per time unit for a predetermined range of the digital input data around a medium value, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding to the digital input data;

an integration circuit for integrating the pulse string generated by the pulse select/synthesis circuit to output a voltage for gamma correction,

wherein the pulse select/ synthesis circuit outputs a logical sum between a carry output from an adder circuit, which has as its inputs high order W bits of the digital input data of n bits and low order W bits of a binary counter, and a logical product between outputs X(m-1) through X(0) of the pulse generation circuit where m=n-W and the digital input data D(m-1) through D(O), and wherein if the digital input data is n bits, then the pulse generation circuit outputs the reference pulses using an n-bit binary counter, an n-1 bit latch, and n-1 2-input gates as claimed in Claim 19.

The present invention is directed to a reference pulse generation circuit for generating reference pulses corresponding to n-bit digital input data, comprising: an n-bit binary counter for counting up in synchronization with an input clock; an n-1 bit latch for generating signals by delaying high order n-1 bits output B (n-1) through B(1) from the binary counter by one input clock period; and n-1 logical circuits for performing logical operations with receiving as inputs the high order n-1 bits output B(n-1) through B(1) from the binary counter and the delayed signals corresponding to the high order n-1 bits output B(n-1) through B(1) from the n-1 bit latch and obtaining outputs X(0)

through X(n-2) with lower reference pulse densities, whereas output X(n-1) is obtained bypassing the logical circuit, wherein the pulse strings comprise a frequency characteristic having a trapezoidal shape corresponding lo the digital input data, and wherein the n-1 logical circuits are n-1 AND circuits, and the n-1 logical circuits are n-2 AND circuits outputting X(0) through X(n-3) and a NOR circuit outputting X(n-2) ad claimed in Claim 20.

The closest prior arts, either singularly or in combination, fail to anticipate or render the above underlined limitations obvious.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VIJAY SHANKAR whose telephone number is (571) 272-7682. The examiner can normally be reached on M-F 7:00 am - 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, BIPIN SHALWALA can be reached on (571) 272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIJAY SHANKAR
Primary Examiner
Art Unit 2673

VS